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PTO/SB/50 (12/97)

REISSUE PATENT APPLICATION TRANSMITTAL

ADDRESS TO:
Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

Attorney Docket No.	2818.1US (92-0399.1-RE)
First Named Inventor	Michael B. Ball
Original Patent No.	5,291,061
Original Patent Issue Date (*Month/Day/Year*)	03/01/94
Express Mail Label No.	EL413915105US

APPLICATION FOR REISSUE OF: (*Check applicable box*) ☒ Utility Patent ☐ Design Patent ☐ Plant Patent

APPLICATION ELEMENTS	ACCOMPANYING APPLICATION PARTS
1. ☒ Fee Transmittal Form (PTO/SB/56) *(Submit an original, and a duplicate for fee processing)*	7. ☒ Transfer drawings from Patent File
2. ☒ Specification and Claims (*amended, if appropriate*)	8. ☐ Foreign Priority Claim (*35 USC 119*) (*if applicable*)
3. ☒ Drawing(s) (*proposed amendments, if appropriate*)	9. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
4. ☒ Reissue Oath or Declaration (*original or copy*) (37 CFR 1.175)(PTO/SB/51 or 52)	10. ☐ English Translation of Reissue Oath/Declaration (*if applicable*)
5. Original U S Patent ☒ Offer to Surrender Original Patent (*37 CFR 1.178*) (*PTO/SB/53 or PTO/SB/54*) or ☐ Ribboned Original Patent Grant ☐ Affidavit/Declaration of Loss (*PTO/SB/55*)	11. ☐ Small Entity ☐ Statement filed in prior application Statement(s) Status still proper and desired
6. Original U.S. Patent currently assigned? ☒ Yes ☐ No (*If Yes, check applicable box(es)*) ☒ Written Consent of all Assignees (*PTO/SB/53 or 54*) ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney	12. ☒ Preliminary Amendment 13. ☒ Return Receipt Postcard (*MPEP 503*) (*Should be specifically itemized*) 14. ☐ Other: . . . . .

15. CORRESPONDENCE ADDRESS

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PTO/SB/56 (12-97)
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REISSUE APPLICATION FEE TRANSMITTAL FORM

Docket Number (Optional): 2818.1US (92-0399.1-RE)

Claims as Filed - Part 1

Claims in Patent	For	Number Filed in Reissue Application	(3) Number Extra	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
(A) 2	Total Claims (37 CFR 1.16(j))	(B) 12	**** 0 =	x $___ =		or	x $ 18 =	0.00
(C) 2	Independent Claims (37 CFR 1.16(i))	(D) 3	* 1 =	x $___ =			x $ 78 =	78.00
				Basic Fee (37 CFR 1.16(h))	$___			$760.00
				Total Filing Fee	$		OR	$838.00

Claims as Amended - Part 2

	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Extra Claims Present	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
Total Claims (37 CFR 1.16(j))	***	MINUS	**	* =	x $___ =		or	x $___ =	
Independent Claims (37 CFR 1.16(i))	***	MINUS	*****	=	x $___ =			x $___ =	
				Total Additional Fee		$		OR	$

* If the entry in (D) is less than the entry in (C), Write "0" in column 3.
** If the "Highest Number of Total Claims Previously Paid For" is less than 20, Write "20" in this space.
*** After any cancelation of claims
**** If "A" is greater than 20, use (B -A); if "A" is 20 or less, use (B - 20).
***** "Highest Number of Independent Claims Previously Paid For" or Number of Independent Claims in Patent (C).

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☒ The Commissioner is hereby authorized to charge any additional fees under 37 CFR 1.16 or 1.17 which may be required, or credit any overpayment to Deposit Account No. 20-1469.
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10/22/99
Date

Brick G. Power
Signature of Applicant, Attorney or Agent of Record

BRICK G. POWER
Typed or printed name

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REISSUE APPLICATION FEE TRANSMITTAL FORM

Docket Number (Optional): 2818.1US (92-0399.1-RE)

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(A) 2	Total Claims (37 CFR 1.16(j))	(B) 12	**** 0 =	x $___ =		or	x $ 18 =	0.00
(C) 2	Independent Claims (37 CFR 1.16(i))	(D) 3	* 1 =	x $___ =			x $ 78 =	78.00
				Basic Fee (37 CFR 1.16(h))	$___			$760.00
				Total Filing Fee	$		OR	$838.00

Claims as Amended - Part 2

	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Extra Claims Present	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
Total Claims (37 CFR 1.16(j))	***	MINUS	**	* =	x $___ =		or	x $___ =	
Independent Claims (37 CFR 1.16(i))	***	MINUS	*****	=	x $___ =			x $___ =	
				Total Additional Fee	$			OR	$

* If the entry in (D) is less than the entry in (C), Write "0" in column 3.
** If the "Highest Number of Total Claims Previously Paid For" is less than 20, Write "20" in this space.
*** After any cancelation of claims
**** If "A" is greater than 20, use (B -A); if "A" is 20 or less, use (B - 20).
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Date

Brick G. Power
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BRICK G. POWER
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:

Ball

U.S. Patent No.: 5,291,061

Issued: March 1, 1994

For: MULTI-CHIP STACKED DEVICES

Attorney Docket No.: 2818US

CERTIFICATE OF MAILING

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02/29/96 Mathew R Allen

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Mathew R. Allen

Typed name of person whose signature is contained above

ASSENT OF ASSIGNEE TO REISSUE

Assistant Commissioner of Patents
BOX PATENT APPLICATIONS
Washington, D.C. 20231

Sir:

The undersigned assignee of the entire interest in U. S. Patent 5,291,061 hereby assents to the accompanying application for reissue of U.S. Patent 5,291,061.

Pursuant to 37 C.F.R. § 3.73, the undersigned representative of the Assignee has reviewed the evidentiary documents, specifically the Assignment to Micron Technology, Inc. recorded on April 6, 1993, at Reel 6513, Frames 0762-0764, and certifies that to the best of his knowledge and belief, title remains in the name of Micron Technology, Inc.

MICRON TECHNOLOGY, INC.

Date: 2-26-96

By: Bryan Farney
W. Bryan Farney
Vice President & General Counsel

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:

Ball

U.S. Patent No.: 5,291,061

Issued: March 1, 1994

For: MULTI-CHIP STACKED DEVICES

Attorney Docket No.: 2818US

CERTIFICATE OF MAILING

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02/29/96 Mathew R Allen

(Signature of person mailing paper)

Mathew R. Allen

(Typed name of person whose signature is given above)

OFFER TO SURRENDER

Assistant Commissioner of Patents
BOX PATENT APPLICATIONS
Washington, D.C. 20231

Sir:

The undersigned applicant of the accompanying reissue application of Letters Patent for "Multi-Chip Stacked Devices", U. S. Patent 5,291,061, granted March 1, 1994, of which Micron Technology, Inc. is now sole owner by assignment, and on whose behalf and with whose assent the accompanying application is made, hereby offers to surrender said Letters Patent.

Pursuant to 37 C.F.R. § 3.73, the undersigned representative of the Assignee has reviewed the evidentiary documents, specifically the Assignment to Micron Technology, Inc. recorded on April 6, 1993, at Reel 6513, Frames 0762-0764, and certifies that to the best of his knowledge and belief, title remains in the name of Micron Technology, Inc.

MICRON TECHNOLOGY, INC.

Date: 2-26-96

By: Bryan Farney m.r.a.
W. Bryan Farney
Vice President & General Counsel

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Michael B. Ball

Serial No.: Not Yet Assigned

Filed: October 22, 1999

For: MULTI-CHIP STACKED DEVICES

Examiner: Unknown

Group Art Unit: Unknown

Attorney Docket No.: 2818.1US
(92-0399.1-RE)

NOTICE OF EXPRESS MAILING
Express Mail Mailing Label Number: EL413915105US
Date of Deposit with USPS: October 22, 1999
Person making Deposit: Jared Turner

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please revise the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Column 1, line 11, insert the following paragraph:

--Cross Reference to Related Application: This reissue application is a continuation of reissue application Serial No. 08/610,127, filed February 29, 1996, pending; which is a reissue application of U.S. Patent No. 5,291,061, dated March 1, 1994.--

IN THE CLAIMS:

Please amend claims 1 and 2 as follows:

1. (Amended) A multiple-die, low-profile semiconductor device comprising:

a. a lead-frame paddle supported by a lead frame;

b. a controlled, first, thin-adhesive layer of about 0.001 inches affixing a first die above the paddle;

c. a plurality of thin wires having a first low-loop wire bond to a plurality of first [diebonding] die-bonding pads, said first wire bond having a wire height above the [bonding pad] first die-bonding pads of about 0.006 inches, and a second wire bond to a plurality of adjacent lead-frame lead fingers;

d. a second thin-adhesive layer of about 0.008 inches affixing a second die above the first die;

e. a second plurality of thin wires having low-loop wire bonds to a plurality of - second die-bonding pads and second wire bonds to the plurality of lead fingers;

f. two additional dies affixed above the second die by additional subsequent layers of adhesive of about 0.008 inches and having additional thin wires bonded to additional bonding pads and lead fingers; and

g. an [encapsulated] encapsulation layer surrounding all dies, adhesive layers, and thin wires wherein a total encapsulated-package height is about 0.110 inches.

2. (Amended) A multiple-die, low-profile semiconductor device comprising:

a. a lead-frame paddle supported by a lead frame;

b. a controlled, first, thin-adhesive layer of about 0.001 to 0.005 inches affixing a first die above the paddle;

c. a plurality of thin wires having a first low-loop wire bond to a plurality of first die-bonding pads, said low-loop wire [ball] bond having a wire height above the first die-bonding pads of about 0.006 inches and a second wire bond to a plurality of adjacent lead-frame lead fingers;

d. a second thin-adhesive layer of about 0.008 to 0.010 inches affixing a second die above the first die;

e. a second plurality of thin wires having low-loop wire bonds to a plurality of second die-bonding pads and second wire bonds to the plurality of lead fingers;

f. an [encapsulated] encapsulation layer surrounding all die adhesive layers and thin wires wherein a total encapsulation-layer height is about 0.070 inches.

REMARKS

No new matter has been added. The Applicant requests entry of the foregoing amendment prior to examination of the application on the merits.

Respectfully submitted,

Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASK, BRITT & ROSSA
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: October 22, 1999

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MULTI-CHIP STACKED DEVICES

FIELD OF THE INVENTION

This invention relates to a multiple die module that has a thickness the same or less than a standard package but has two or more stacked die, thereby increasing device density.

BACKGROUND OF THE INVENTION

Semiconductor devices are typically constructed en masse on a silicon or gallium arsenide wafer through a process which comprises a number of deposition, masking, diffusion, etching, and implanting steps. When the devices are sawed into individual rectangular units, each takes the form of an integrated circuit (IC) die. In order to interface a die with other circuitry, it is (using contemporary conventional packaging technology) mounted on a lead frame paddle of a lead-frame strip which consists of a series of interconnected lead frames, typically ten in a row. The die-mounting paddle of a standard lead frame is larger than the die itself, and it is surrounded by multiple lead fingers of individual leads. The bonding pads of the die are then connected one by one in a wire-bonding operation to the lead frame's lead finger pads with extremely fine gold or aluminum wire. Following the application of a protective layer to the face of the die, it, and a portion of the lead frame to which it is attached, is encapsulated in a plastic material, as are all other die/lead-frame assemblies on the lead-frame strip. A trim-and-form operation then separates the resultant interconnected packages and bends the leads of each package into the proper configuration.

In the interest of higher performance equipment and lower cost, increased miniaturization of components and greater packaging density have long been the goals of the computer industry. IC package density is primarily limited by the area available for die mounting and the height of the package. Typical computer-chip heights in the art are about 0.110 inches. A method of increasing density is to stack die or chips vertically.

U.S. Pat. No. 5,012,323, issued Apr. 30, 1991, having a common assignee with the present application, discloses a pair of rectangular integrated-circuit dice mounted on opposite sides of the lead frame. An upper, smaller die is back-bonded to the upper surface of the lead fingers of the lead frame via a first adhesively coated, insulated film layer. The lower, slightly larger die is face-bonded to the lower surface of the lead extensions within the lower lead-frame die-bonding region via a second, adhesively coated, insulative, film layer. The wire-bonding pads on both upper die and lower die are interconnected with the ends of their associated lead extensions with gold or aluminum wires. The lower die needs to be slightly larger in order that the die pads are accessible from above so that gold wire connections can be made to the lead extensions (fingers).

U.S. Pat. No. 4,996,587 (referred to hereafter as '587) shows a semiconductor chip package which uses a chip carrier to support the chips within a cavity. The chip carrier as shown in the figures has a slot that permits connection by wires to bonding pads which, in turn, connect to the card connector by conductors. An encapsulation material is placed only on the top surface of the chip in order to provide heat dissipation from the bottom surface when carriers are stacked.

A Japanese Patent No. 56-62351(A) issued to Sano in 1981 discloses three methods of mounting two chips on

a lead frame and attaching the pair of semiconductor chips (pellets) to a common lead frame consisting of:

method 1 two chips mounted on two paddles;

method 2 one chip mounted over a paddle and one below not attached to the paddle; and

method 3 one chip attached above and one chip attached below a common paddle.

The chips are apparently wired in parallel as stated in the "PURPOSE" of Sano.

The chips of patent '587 are also apparently wired in parallel by contacts on the "S" chips which contact the connection means.

It is the purpose of this invention to provide multiple stacked dies assembled in a special vertical configuration such that as many as four encapsulated dies will have a height no greater than existing 0.110-inch high dies and also have a separate lead and lead finger for each die pad connection.

SUMMARY OF THE INVENTION

The invention generally stated is a multiple-die low-profile semiconductor device comprising:

a lead-frame paddle supported by a lead frame;

a controlled, first, thin-adhesive layer affixing a first die above the paddle;

a plurality of thin wires having a first low-loop wire bond to a plurality of first die-bonding pads and a second wire bond to a plurality of adjacent lead-frame lead fingers;

a second thin-adhesive layer affixing a second die above the first die;

a second plurality of thin wires having low-loop wire bonds to a plurality of second die-bonding pads and second wire bonds to the plurality of lead fingers;

additional dies affixed above the second die, by additional subsequent layers of adhesive and having additional thin wires bonded to addition bonding pads and lead fingers; and

an encapsulated layer surrounding all dies, adhesive layers, and thin wires.

Other objects, advantages, and capabilities of the present invention will become more apparent as the description proceeds.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be better understood and further advantages and uses thereof may become more readily apparent when considered in view of the following detailed description of exemplary embodiments, taken with the accompanied drawings, in which:

FIG. 1 is a partial plan view of the stacked die, lead fingers, and bonded wires of the present invention; and

FIG. 2 is a side elevation taken through lines 2—2 of FIG. 1 showing a four die stacking.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, the stacked die device 10 is shown priot to encapsulation disclosing the top die 12 mounted the paddle 14 and other dies 16, 18, and 20 (FIG. 2) which are adhesively connected to each other by a controlled-thickness thermoplastic-adhesive layer at 22. Thermoplastic indicating the adhesive sets at an elevated temperature. The group of four dies are attached to the paddle 14 by a controlled thin-adhesive layer 24.

Each of the die bonding pads 26 in double rows are electrically connected to multiple lead fingers 28A, 28B, 28C . . . 28N by thin (0.001 inch) gold or aluminum wires 30A, 30B, 30C . . . 30N; gold being the preferred metal. For clarity, only part of the 18 bonding pads, wires, and fingers are shown. The critical bonding method used at the die end pad 26 is an ultrasonic ball bond as named by the shape of the bond as at 32. This first-installed bond and formed gold wire are low-loop wire bonds as seen at critical dimension 34, as will be described later.

The other end of gold wires 30 are attached to the lead fingers by a wedge bond 36, which is also an ultrasonic bond, indicating the use of ultrasonic energy to heat the wire 30 as it is compressed against the lead finger 28. The wedge bond is not used on the die because the bonding machine contacts the bonding surface and could damage this critical surface. The lead fingers may be formed upward as at 38 to permit the use of shorter wires 30.

Paddle 14 which supports the stack is attached to the lead frame typically at four corners as at 40 and also typically, in this application, would have a downset from the lead frame and lead fingers 28 as at dimension 42. The stack is finally encapsulated by a plastic or ceramic at 44.

A dimensional analysis is provided by referring to FIG. 2.

By careful control of layer thicknesses, it is possible to fabricate a four-stack die device having an overall height 46 of about 0.110 inches which is the same height as a current single die. Starting at the bottom, the encapsulation thickness 48 is between 0.010 and 0.012 inches. The paddle 74 thickness 50 can be between 0.005 and 0.010 inches and is a matter of choice. The controlled adhesive-layer thickness 52 can be from 0.001 to 0.005 inches. The individual dies 20, 18, 16, and 12 each have a thickness 54 of 0.012 inches and the critical controlled, adhesive-layer thicknesses 56 between each die are between 0.008 and 0.010 inches. These thin layers have to be slightly greater than the low-loop wire dimension 34, which is about 0.006 inches. Finally, the top encapsulation thickness 58 is between 0.010 and 0.012 inches so as to cover the top loop.

Thus, it can be seen by carefully controlling and minimizing the adhesive layer thicknesses 56, the top and bottom encapsulation thicknesses 48 and 58, and the paddle adhesive layer 52 that it is possible to have an overall height between 0.108 and 0.110 inches overall for the four-stack die.

If the looser tolerances were used for a two-stack die, the height at 60 would be between 0.058 and 0.073 inches and for a three-die stack it would be from 0.078 to 0.100 inches.

The fabrication of these two or four-stack die devices, necessarily, has to be from the bottom up, since it is not possible to form the die pad wire ball bond 32 on the lower dies 16, 18, and 30, if the four dies are already stacked. This is due to the overhead space required by the wire bond machine.

The die pads 26 of each die can be each connected to an individual lead finger 28 or the dies can be wired in parallel. The former configuration would, therefore,

require (for a four die stack) something less than $4 \times 18 = 72$ leads, while parallel connections would require something on the order of 22 or more pins, depending on the type of devices and system requirements. The final packages can be in the form of a small outline J-leaded (SOJ) package, a dual in-line package (DIP), a single in-line package (SIP), a plastic leaded chip carrier (PLCC), and a zig-zag in-line package (ZIP).

While a preferred embodiment of the invention has been disclosed, various modes of carrying out the principles disclosed herein are contemplated as being within the scope of the following claims. Therefore, it is understood that the scope of the invention is not to be limited except as otherwise set forth in the claims.

What is claimed is:

1. A multiple-die low-profile semiconductor device comprising:

a. a lead-frame paddle supported by a lead frame;

b. a controlled, first, thin-adhesive layer of about 0.001 inches affixing a first die above the paddle;

c. a plurality of thin wires having a first low-loop wire bond to a plurality of first diebonding pads, said wire bond having a wire height above the bonding pad of about 0.006 inches, and a second wire bond to a plurality of adjacent lead-frame lead fingers;

d. a second thin-adhesive layer of about 0.008 inches affixing a second die above the first die;

e. a second plurality of thin wires having low-loop wire bonds to a plurality of second die-bonding pads and second wire bonds to the plurality of lead fingers;

f. two additional dies affixed above the second die by additional subsequent layers of adhesive of about 0.008 inches and having additional thin wires bonded to additional bonding pads and lead fingers; and

g. an encapsulated layer surrounding all dies, adhesive layers, and thin wires wherein a total encapsulated-package height is about 0.110 inches.

2. A multiple-die low-profile semiconductor device comprising:

a. a lead-frame paddle supported by a lead frame;

b. a controlled, first, thin-adhesive layer of about 0.001 to 0.005 inches affixing a first die above the paddle;

c. a plurality of thin wires having a first low-loop wire bond to a plurality of first die-bonding pads, said low-loop wire ball bond having a wire height above the bonding pads of about 0.006 inches and a second wire bond to a plurality of adjacent lead-frame lead fingers;

d. a second thin-adhesive layer of about 0.008 to 0.010 inches affixing a second die above the first die;

e. a second plurality of thin wires having low-loop wire bonds to a plurality of second die-bonding pads and second wire bonds to the plurality of lead fingers;

f. an encapsulated layer surrounding all die adhesive layers and thin wires wherein a total encapsulation-layer height is about 0.070 inches.

* * * * *

3. A method for fabricating a multiple-die, low-profile semiconductor device, comprising:

a. providing a lead frame having a lead frame paddle and a plurality of lead fingers;

b. affixing to said paddle a first die having a plurality of first die-bonding pads;

c. connecting bond wires between each of said plurality of first die-bonding pads and corresponding lead fingers of said plurality of lead fingers by way of a low-loop wire bond on each of said plurality of first die-bonding pads and a wire bond on each of said corresponding lead fingers;

d. affixing to said first die, following said connecting bond wires, a second die having a plurality of second die-bonding pads;

e. connecting bond wires between each of said plurality of second die-bonding pads and corresponding lead fingers of said plurality of lead fingers by way of a low-loop wire bond on each of said plurality of second die-bonding pads and a wire bond on each of said corresponding lead fingers; and

f. affixing two additional dies above said second die.

4. The method of claim 3, further comprising encapsulating all dies and bond wires with an encapsulation layer having a height of about 0.110 inches.

5. The method of claim 3, wherein die-bonding pads of said first plurality of die-bonding pads are connected to said corresponding lead fingers of said plurality of lead fingers in parallel with die-bonding pads of said second plurality of die-bonding pads.

6. The method of claim 3, wherein die-bonding pads of said first plurality of die-bonding pads and die-bonding pads of said second plurality of die-bonding pads are each connected to individual ones of said plurality of lead fingers.

7. The method of claim 3, wherein said providing comprises providing a lead frame having a downset lead frame paddle and a plurality of lead fingers upset relative to said downset lead frame paddle.

8. The method of claim 3, wherein said connecting bond wires between each of said first and second pluralities of die-bonding pads and corresponding ones of said lead fingers comprises forming said low-loop wire bonds on each of said die-bonding pads to be ball bonds.

9. The method of claim 3, wherein said connecting bond wires between each of said first and second pluralities of die-bonding pads and corresponding ones of said lead fingers comprises forming said wire bonds on each of said corresponding lead fingers to be wedge bonds.

10. The method of claim 3, wherein said affixing said first die to said lead frame paddle comprises disposing a layer of adhesive between said lead frame paddle and said first die.

11. The method of claim 10, wherein said disposing said layer of adhesive comprises forming said layer of adhesive to be about 0.001 inches thick.

12. The method of claim 3, wherein said affixing said second die to said first die comprises disposing a layer of adhesive between said first die and said second die.

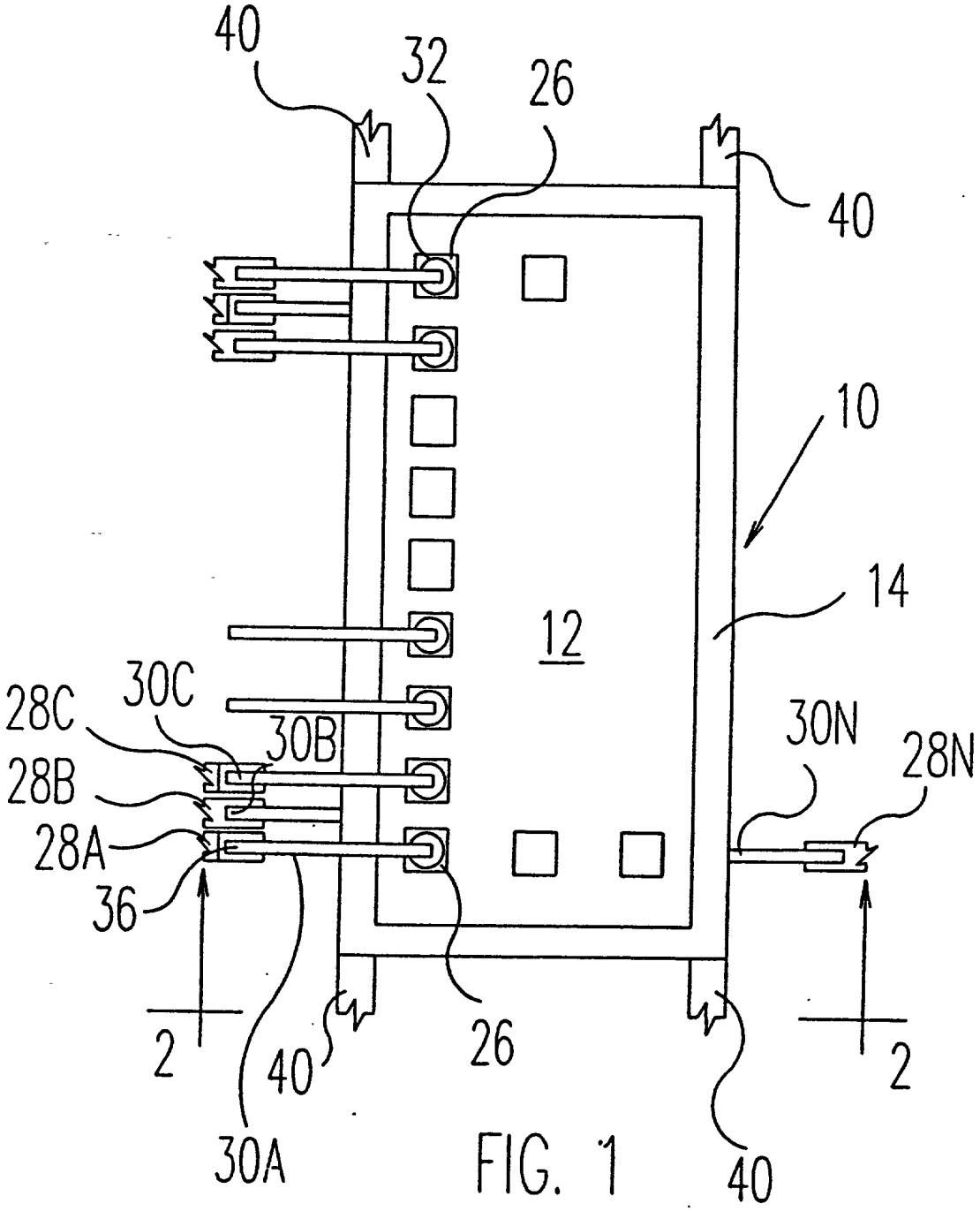

FIG. 1

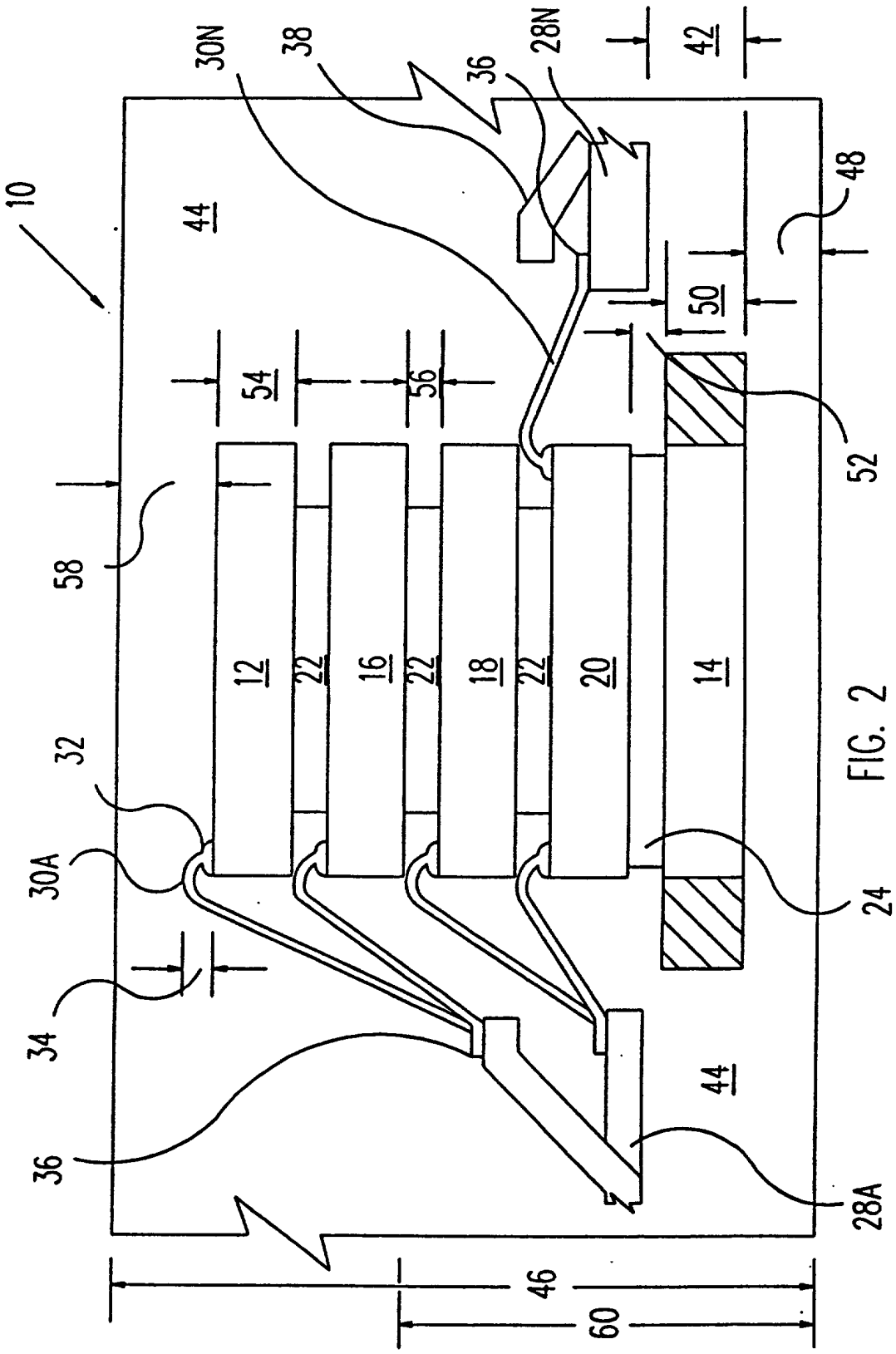
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FIG. 2

PTO/SB/51 (12-97)
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REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) 2818.1US (92-0399.1-RE)

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is described and claimed in patent number 5,291,061, granted March 1, 1994, and for which a reissue patent is sought on the invention entitled MULTI-CHIP STACKED DEVICES

the specification of which

[X] is attached hereto.

[ ] was filed on _____ as reissue application number ___ / _____
and was amended on _____ .
(If applicable)

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.
I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

[ ] by reason of a defective specification or drawing.

[X] by reason of the patentee claiming more or less than he had the right to claim in the patent.

[ ] by reason of other errors.

At least one error upon which reissue is based is described as follows:

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(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)
2818.1US (92-0399.1-RE)

All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant. As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

Full name of sole or first inventor (given name, family name)
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Inventor's signature Michael B Ball

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Full name of second joint inventor (given name, family name)

Inventor's signature	Date
Residence	Citizenship
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Full name of third joint inventor (given name, family name)

Inventor's signature	Date
Residence	Citizenship
Post Office Address	

☐ Additional joint inventors are named on separately numbered sheets attached hereto.